Application Report
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UCC28950 600-W, Phase-Shifted, Full-Bridge Application Report

Michael O'Loughlin

Introduction

In high-power server applications to meet high-efficiency and green standards some power-supply designers have found it easier to use a phase-shifted, full-bridge converter. This is because the phase-shifted, full-bridge converter can obtain zero-voltage switching on the primary side of the converter reducing switching losses, and EMI and increasing overall efficiency. The purpose of this application report is to review the design of the 600-W, phase-shifted, full-bridge converter for one of these power systems, using TI's new UCC28950 Phase-Shifted, Full-Bridge Controller, and was based on typical values. In a production design the values need to be modified for worst case conditions. Hopefully this information will aid other power supply designers in their efforts to design an efficient phase-shifted, full-bridge converter. Also note there is a MathCAD Design Tool, (TI Literature Number SLUC210), that goes along with this application note as well.

Design Specifications

DESCRIPTION	MIN	TYP	MAX
Input Voltage	370 V (V_{INMIN})	390 V (V_{IN})	410 V (V_{INMAX})
Output Voltage	11.4 V	12 V (V_{OUT})	12.6 V
Allowable Output Voltage Transient			600 mV (V_{TRAN})
Load Step, 90%			
Output Power			600 W (P_{OUT})
Full Load Efficiency	93% (η)		
Inductor (L_{OUT}) Switching Frequency		200 kHz (f_S)	

Functional Schematic

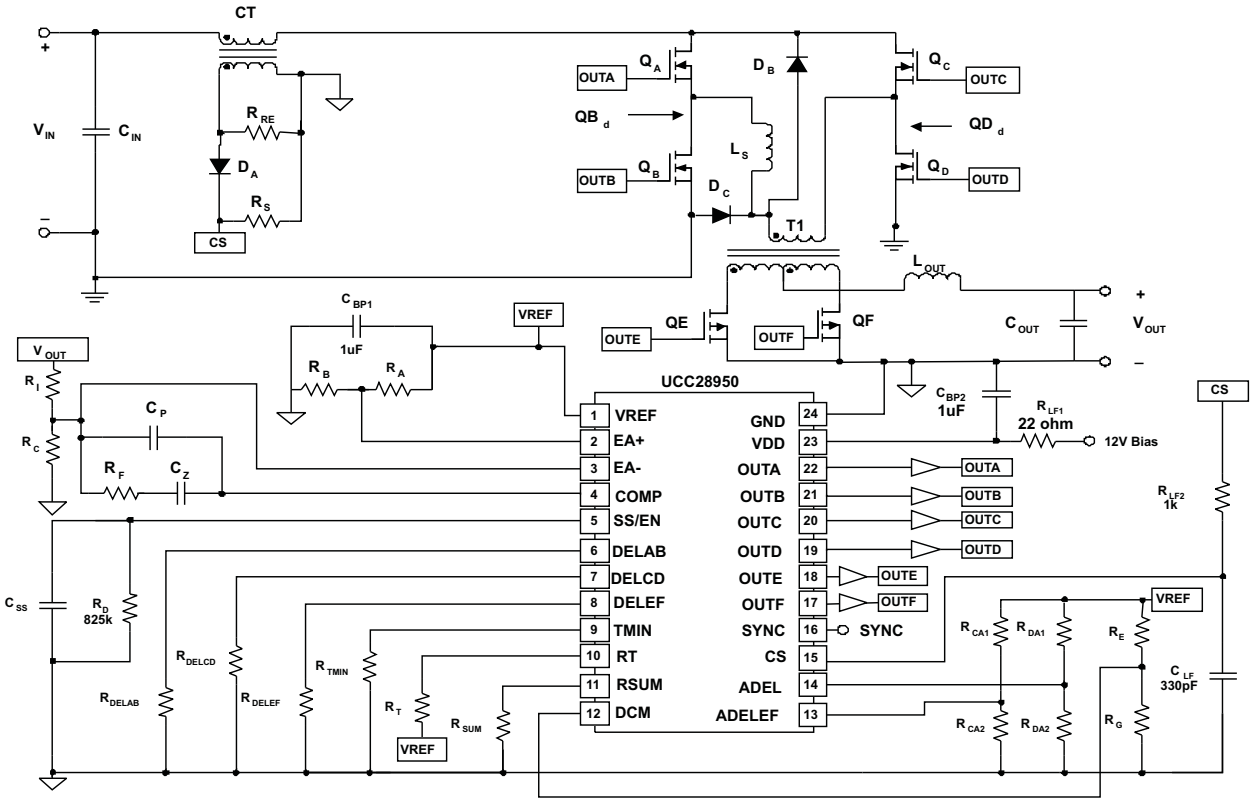

Figure 1. UCC28950 Phase-Shifted, Full-Bridge Functional Schematic

Power Budget

To meet the efficiency goal a power budget needs to be set.

$$P_{BUDGET} = P_{OUT} \times \left(\frac{1-\eta}{\eta} \right) \approx 45.2\,W \tag{1}$$

Preliminary Transformer Calculations (T1)

Transformer turns ratio (a1):

$$a1 = \frac{N_P}{N_S} \tag{2}$$

Estimated FET voltage drop (V_{RDSON}):

$$V_{RDSON} = 0.3\,V \tag{3}$$

Select transformer turns based on 70% duty cycle (D_{MAX}) at minimum specified input voltage. This will give some room for dropout if a PFC front end is used.

$$a1 = \frac{N_P}{N_S} \tag{4}$$

$$a1 = \frac{(V_{INMIN} - 2 \times V_{RDSON}) \times D_{MAX}}{V_{OUT} + V_{RDSON}} \approx 21 \tag{5}$$

Turns ratio rounded to the nearest whole turn.

$$a1 = 21 \tag{6}$$

Calculated typical duty cycle (D_{TYP}) based on average input voltage.

$$D_{TYP} = \frac{(V_{OUT} + V_{RDSON}) \times a}{(V_{IN} - 2 \times V_{RDSON})} \approx 0.66 \tag{7}$$

Output inductor ripple current is set to 20% of the output current.

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = 10\,A \tag{8}$$

Care needs to be taken in selecting a transformer with the correct amount of magnetizing inductance (L_{MAG}). The following equations calculate the minimum magnetizing inductance of the primary of the transformer (T1) to ensure the converter operates in current-mode control. If L_{MAG} is too small the magnetizing current could cause the converter to operate in voltage mode control instead of peak-current mode control. This is because the magnetizing current is too large, it will act as a PWM ramp swamping out the current sense signal across R_S.

$$L_{MAG} \geq \frac{V_{IN} \times (1 - D_{TYP})}{\frac{\Delta I_{LOUT} \times 0.5}{a1} \times f_S} \approx 2.76\,mH \tag{9}$$

Figure 2 shows T1 primary current ($I_{PRIMARY}$) and synchronous rectifiers QE (I_{QE}) and QF (I_{QF}) currents with respect to the synchronous rectifier gate drive currents. Note that I_{QE} and I_{QF} are also T1's secondary winding currents as well. Variable D is the converters duty cycle.

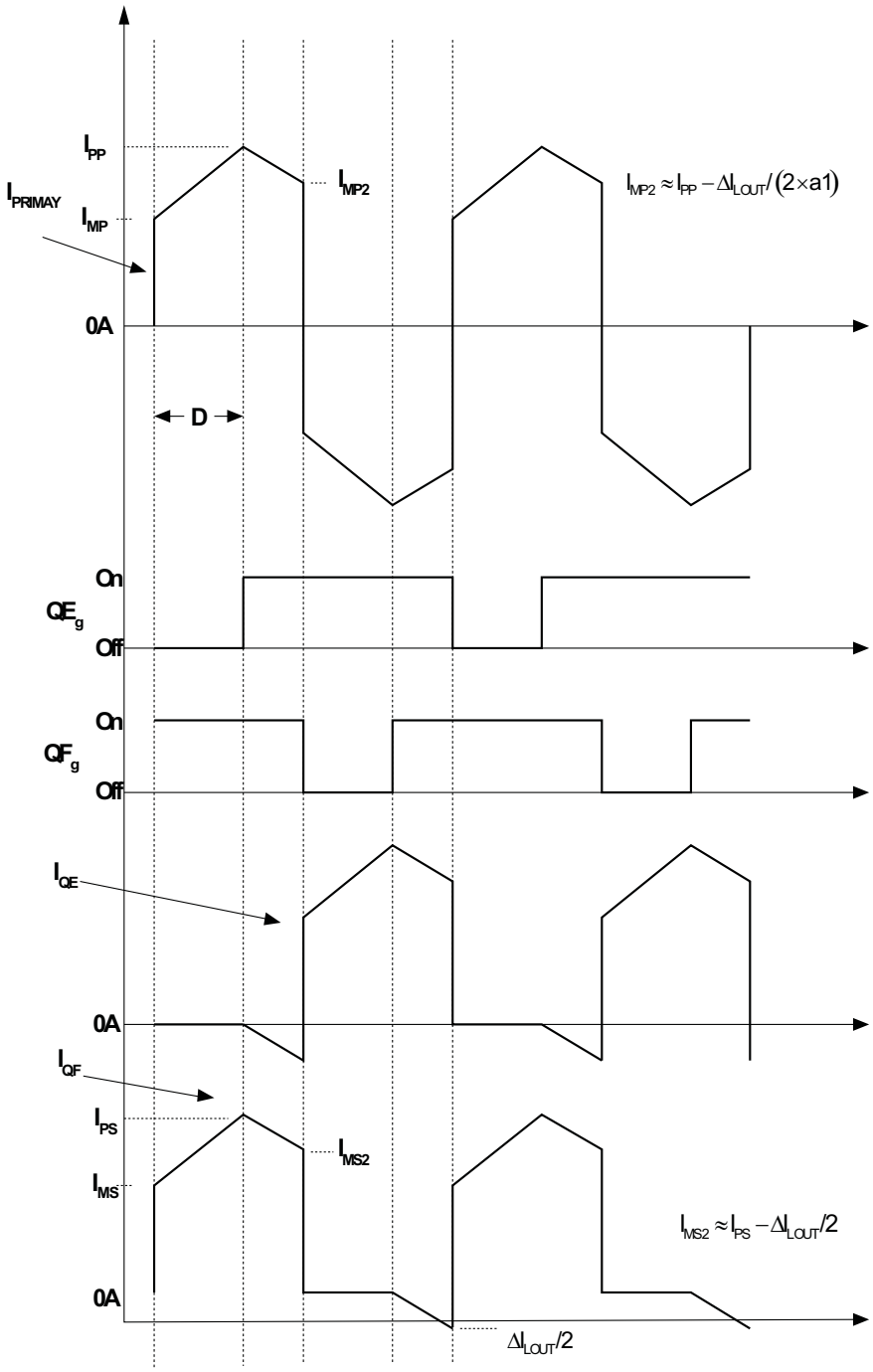

Figure 2. T1 Primary and QE and QF FET Currents

Calculate T1 secondary RMS current (I_{SRMS}):

$$I_{PS} = \frac{P_{OUT}}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2} \approx 55\,A \tag{10}$$

$$I_{MS} = \frac{P_{OUT}}{V_{OUT}} - \frac{\Delta I_{LOUT}}{2} \approx 45\,A \tag{11}$$

$$I_{MS2} = I_{PS} - \frac{\Delta I_{LOUT}}{2} \approx 50\,A \tag{12}$$

Secondary RMS current (I_{SRMS1}) when energy is being delivered to the secondary:

$$I_{SRMS1} = \sqrt{\left(\frac{D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS} + \frac{\left(I_{PS} - I_{MS}\right)^2}{3}\right]} \approx 29.6\,A \tag{13}$$

Secondary RMS current (I_{SRMS2}) when current is circulating through the transformer when QE and QF are both on.

$$I_{SRMS2} = \sqrt{\left(\frac{1-D_{MAX}}{2}\right)\left[I_{PS} \times I_{MS2} + \frac{\left(I_{PS} - I_{MS2}\right)^2}{3}\right]} \approx 20.3\,A \tag{14}$$

Secondary RMS current (I_{SRMS3}) caused by the negative current in the opposing winding during freewheeling period, please refer to Figure 2.

$$I_{SRMS3} = \frac{\Delta I_{LOUT}}{2}\sqrt{\left(\frac{1-D_{MAX}}{2\times 3}\right)} \approx 1.1A \tag{15}$$

Total secondary RMS current (I_{SRMS}):

$$I_{SRMS} = \sqrt{I_{SRMS1}^{\,2} + I_{SRMS2}^{\,2} + I_{SRMS3}^{\,2}} \approx 36.0\,A \tag{16}$$

Calculate T1 Primary RMS Current (I_{PRMS}):

$$\Delta I_{LMAG} = \frac{V_{INMIN} \times D_{MAX}}{L_{MAG} \times f_S} \approx 0.47\,A \tag{17}$$

$$I_{PP} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} + \Delta I_{LMAG} \approx 3.3\,A \tag{18}$$

$$I_{PRMS1} = \sqrt{(D_{MAX})\left[I_{PP} \times I_{MP} + \frac{\left(I_{PP} - I_{MP}\right)^2}{3}\right]} \approx 2.5\,A \tag{19}$$

$$I_{MP2} = I_{PP} - \left(\frac{\Delta I_{LOUT}}{2}\right)\frac{1}{a1} \approx 3.0\,A \tag{20}$$

T1 Primary RMS (I_{PRMS1}) current when energy is being delivered to the secondary.

$$I_{PRMS1} = \sqrt{(D_{MAX})\left[I_{PP} \times I_{MP} + \frac{(I_{PP} - I_{MP})^2}{3}\right]} \approx 2.5\,A \quad (21)$$

T1 Primary RMS (I_{PRMS2}) current when the converter is free wheeling.

$$I_{PRMS2} = \sqrt{(1 - D_{MAX})\left[I_{PP} \times I_{MP2} + \frac{(I_{PP} - I_{MP2})^2}{3}\right]} \approx 1.7\,A \quad (22)$$

Total T1 primary RMS current (I_{PRMS})

$$I_{PRMS} = \sqrt{I_{PRMS1}^{\ 2} + I_{PRMS2}^{\ 2}} \approx 3.1A \quad (23)$$

For this design a Vitec transformer was selected part number 75PR8107 that had the following specifications.

$$a1 = 21 \quad (24)$$

$$L_{MAG} = 2.8\,mH \quad (25)$$

Measure leakage inductance on the Primary:

$$L_{LK} = 4\,\mu H \quad (26)$$

Transformer Primary DC resistance:

$$DCR_P = 0.215\,\Omega \quad (27)$$

Transformer Secondary DC resistance:

$$DCR_S = 0.58\,\Omega \quad (28)$$

Estimated transform losses (P_{T1}) are twice the copper loss.

NOTE: This is just an estimate and the total losses may vary based on magnetic design.

$$P_{T1} \approx 2 \times \left(I_{PRMS}^{\ 2} \times DCR_P + 2 \times I_{SRMS}^{\ 2} \times DCR_S\right) \approx 7.0\,W \quad (29)$$

Calculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{T1} \approx 38.1W \quad (30)$$

QA, QB, QC, QD FET Selection

In this design to meet efficiency and voltage requirements 20 A, 650 V, CoolMOS FETs from Infineon were chosen for QA..QD.

FET drain to source on resistance:

$$R_{ds(on)QA} = 0.220\,\Omega \tag{31}$$

FET Specified C_{OSS}:

$$C_{OSS\_QA\_SPEC} = 780\,pF \tag{32}$$

Voltage across drain-to-source (V_{dsQA}) where C_{OSS} was measured, data sheet parameter:

$$V_{dsQA} = 25\,V \tag{33}$$

Calculate average C_{oss} [2]:

$$C_{OSS\_QA\_AVG} = C_{OSS\_QA\_SPEC}\sqrt{\frac{V_{dsQA}}{V_{INMAX}}} \approx 193\,pF \tag{34}$$

QA FET gate charge:

$$QA_g = 15\,nC \tag{35}$$

Voltage applied to FET gate to activate FET:

$$V_g = 12\,V \tag{36}$$

Calculate QA losses (P_{QA}) based on $R_{ds(on)QA}$ and gate charge (QA_g):

$$P_{QA} = I_{PRMS}{}^2 \times R_{ds(on)QA} + 2 \times QA_g \times V_g \times \frac{fs}{2} \approx 2.1W \tag{37}$$

Recalculate power budget:

$$P_{BUDGET} = P_{BUDGET} - 4 \times P_{QA} \approx 29.7\,W \tag{38}$$

Selecting L_S

Calculating the shim inductor (L_S) is based on the amount of energy required to achieve zero voltage switching. This inductor needs to able to deplete the energy from the parasitic capacitance at the switch node. The following equation selects L_S to achieve ZVS at 100% load down to 50% load based on the primary FET's average total C_{OSS} at the switch node.

NOTE: There may be more parasitic capacitance than was estimated at the switch node and L_S may have to be adjusted based on the actual parasitic capacitance in the final design.

$$L_S \geq \left(2 \times C_{OSS\_QA\_AVG}\right) \frac{V_{INMAX}^{\ 2}}{\left(\frac{I_{PP}}{2} - \frac{\Delta I_{LOUT}}{2 \times a1}\right)^2} - L_{LK} \approx 26\,\mu H \tag{39}$$

For this design a 26-µH Vitec inductor was chosen for L_S, part number 60PR964. The shim inductor had the following specifications.

$$L_S = 26\,\mu H \tag{40}$$

L_S DC Resistance:

$$DCR_{LS} = 27\,m\Omega \tag{41}$$

Estimate L_S power loss (P_{LS}) and readjust remaining power budget:

$$P_{LS} = 2 \times I_{PRMS}^{\ 2} \times DCR_{LS} \approx 0.5\,W \tag{42}$$

$$P_{BUDGET} = P_{BUDGET} - P_{LS} \approx 29.2\,W \tag{43}$$

Output Inductor Selection (L_{OUT})

Inductor L_{OUT} was designed for 20% inductor ripple current (ΔI_{LOUT}):

$$\Delta I_{LOUT} = \frac{P_{OUT} \times 0.2}{V_{OUT}} = \frac{600\,W \times 0.2}{12\,V} \approx 10\,A \tag{44}$$

$$L_{OUT} = \frac{V_{OUT} \times (1 - D_{TYP})}{\Delta I_{LOUT} \times f_s} \approx 2\,\mu H \tag{45}$$

Calculate output inductor RMS current (I_{LOUT_RMS}):

$$I_{LOUT\_RMS} = \sqrt{\left(\frac{P_{OUT}}{V_{OUT}}\right)^2 + \left(\frac{\Delta I_{LOUT}}{\sqrt{3}}\right)^2} = 50.3\,A \tag{46}$$

A 2-µH inductor from Vitec Electronics Corporation, part number 75PR108, was chosen for this design. The inductor had the following specifications.

$$L_{OUT} = 2\,\mu H \tag{47}$$

Output inductor DC resistance:

$$DCR_{LOUT} = 750\,\mu\Omega \tag{48}$$

Estimate output inductor losses (P_{LOUT}) and recalculate power budget. Note P_{LOUT} is an estimate of inductor losses that is twice the copper loss. Note this may vary based on magnetic manufactures. It is advisable to double check the magnetic loss with the magnetic manufacture.

$$P_{LOUT} = 2 \times I_{LOUT\_RMS}{}^2 \times DCR_{LOUT} \approx 3.8\,W \tag{49}$$

$$P_{BUDGET} = P_{BUDGET} - P_{LOUT} \approx 25.4\,W \tag{50}$$

Output Capacitance (C_{OUT})

The output capacitor is being selected based on holdup and transient (V_{TRAN}) load requirements.

Time it takes L_{OUT} to change 90% of its full load current:

$$t_{HU} = \frac{\frac{L_{OUT} \times P_{OUT} \times 0.9}{V_{OUT}}}{V_{OUT}} = 7.5\,\mu s \tag{51}$$

During load transients most of the current will immediately go through the capacitors equivalent series resistance (ESR_{COUT}). The following equations are used to select ESR_{COUT} and C_{OUT} based on a 90% load step in current. The ESR is selected for 90% of the allowable transient voltage (V_{TRAN}), while the output capacitance (C_{OUT}) is selected for 10% of V_{TRAN}.

$$ESR_{COUT} \le \frac{V_{TRAN} \times 0.9}{\frac{P_{OUT} \times 0.9}{V_{OUT}}} = 12\,m\Omega \tag{52}$$

$$C_{OUT} \ge \frac{\frac{P_{OUT} \times 0.9 \times t_{HU}}{V_{OUT}}}{V_{TRAN} \times 0.1} \approx 5.6\,mF \tag{53}$$

Before selecting the output capacitance it is also required to calculate the output capacitor RMS current (I_{COUT_RMS}).

$$I_{COUT\_RMS} = \frac{\Delta I_{LOUT}}{\sqrt{3}} \approx 5.8\,A \tag{54}$$

To meet our design requirements five 1500-µF, aluminum electrolytic capacitors were chosen for the design from United Chemi-Con, part number EKY-160ELL152MJ30S. These capacitors had an ESR of 31 mΩ.

Number of output capacitors:

$$n = 5 \tag{55}$$

Total output capacitance:

$$C_{OUT} = 1500\,\mu F \times n \approx 7500\,\mu F \tag{56}$$

Effective output capacitance ESR:

$$ESR_{COUT} = \frac{31\,m\Omega}{n} = 6.2\,m\Omega \tag{57}$$

Calculate output capacitor loss (P_{COUT}):

$$P_{COUT} = I_{COUT\_RMS}{}^2 \times ESR_{COUT} \approx 0.21\,W \tag{58}$$

Recalculate remaining Power Budget:

$$P_{BUDGET} = P_{BUDGET} - P_{COUT} \approx 25.2\,W \tag{59}$$

Select FETs QE and QF

Selecting FETs for a design is always trial and error. To meet the power requirements of this design we selected 75-V, 120-A FETs, from Fairchild, part number FDP032N08. These FETs' had the following characteristics.

$$QE_g = 152\,nC \tag{60}$$

$$R_{ds(on)QE} = 3.2\,m\Omega \tag{61}$$

Calculate average FET C_{OSS} ($C_{OSS\_QE\_AVG}$) based on the data sheet parameters for C_{OSS} (C_{OSS_SPEC}), and drain to source voltage where C_{OSS_SPEC} was measured (V_{ds_spec}), and the maximum drain to source voltage in the design (V_{dsQE}) that will be applied to the FET in the application.

Voltage across FET QE and QF when they are off:

$$V_{dsQE} = \frac{V_{INMAX}}{a1} \approx 19.5\,V \tag{62}$$

Voltage where FET C_{OSS} is specified and tested in the FET data sheet:

$$V_{ds\_spec} = 25\,V \tag{63}$$

Specified output capacitance from FET data sheet:

$$C_{OSS\_SPEC} = 1810\,pF \tag{64}$$

Average QE and QF C_{OSS} [2]:

$$C_{OSS\_QE\_AVG} = C_{OSS\_SPEC}\sqrt{\frac{V_{dsQE}}{V_{ds\_spec}}} \approx 1.6\,nF \tag{65}$$

QE and QF RMS current:

$$I_{QE\_RMS} = I_{SRMS} = 36.0\,A \tag{66}$$

To estimate FET switching loss the V_g vs. Q_g curve from the FET data sheet needs to be studied. First the gate charge at the beginning of the miller plateau needs to be determined (QE_{MILLER_MIN}) and the gate charge at the end of the miller plateau (QE_{MILLER_MAX}) for the given V_{DS}.

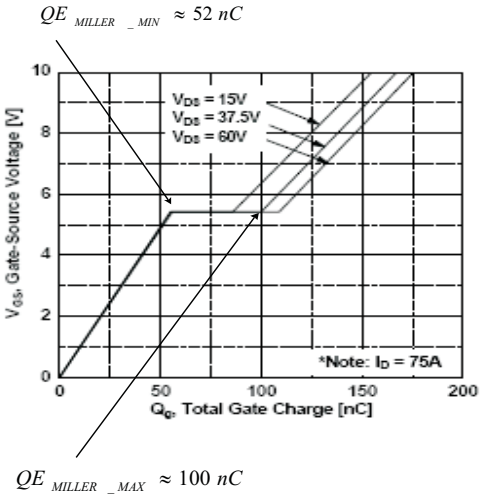

Figure 3. V_g vs. Q_g for QE and QF FETs

Maximum gate charge at the end of the miller plateau:

$$QE_{MILLER\_MAX} \approx 100\,nC \tag{67}$$

Minimum gate charge at the beginning of the miller plateau:

$$QE_{MILLER\_MIN} \approx 52\,nC \tag{68}$$

NOTE: The FETs in this design were driven with UCC27324 setup to drive 4-A (I_P) of gate drive current.

$$I_P \approx 4\,A \tag{69}$$

Estimated FET V_{ds} rise and fall time:

$$t_r \approx t_f = \frac{100nC - 52nC}{\frac{I_P}{2}} = \frac{48nC}{\frac{4A}{2}} \approx 24\,ns \tag{70}$$

Estimate QE and QF FET Losses (P_{QE}):

$$P_{QE} = I_{QE\_RMS}{}^2 \times R_{ds(on)QE} + \frac{P_{OUT}}{V_{OUT}} \times V_{dsQE}\left(t_r + t_f\right)\frac{f_s}{2} + 2 \times C_{OSS\_QE\_AVG} \times V_{dsQE}{}^2 \frac{f_s}{2} + 2 \times Q_{gQE} \times V_{gQE} \frac{f_s}{2} \tag{71}$$

$$P_{QE} \approx 9.3\,W \tag{72}$$

Recalculate the power budget.

$$P_{BUDGET} = P_{BUDGET} - 2 \times P_{QE} \approx 6.5\,W \tag{73}$$

Input Capacitance (C_{IN})

If this converter was designed for a 390-V input, which is generally fed by the output of a PFC boost pre-regulator. The input capacitance is generally selected based on holdup and ripple requirements.

NOTE: The delay time needed to achieve ZVS can act as a duty cycle clamp (D_{CLAMP}).

Calculate tank frequency:

$$f_R = \frac{1}{2\pi\sqrt{L_S \times (2 \times C_{OSS\_QA\_AVG})}} \tag{74}$$

Estimated delay time:

$$t_{DELAY} = \frac{2}{f_R \times 4} \approx 314\,ns \tag{75}$$

Effective duty cycle clamp (D_{CLAMP}):

$$D_{CLAMP} = \left(\frac{1}{fs} - t_{DELAY}\right) \times fs = 94\% \tag{76}$$

V_{DROP} is the minimum input voltage where the converter can still maintain output regulation. The converter's input voltage would only drop down this low during a brownout or line-drop condition if this converter was following a PFC pre-regulator.

$$V_{DROP} = \left(\frac{2 \times D_{CLAMP} \times V_{RDSON} + a1 \times (V_{OUT} + V_{RDSON})}{D_{CLAMP}}\right) = 276.2\,V \tag{77}$$

C_{IN} was calculated based on one line cycle of holdup:

$$C_{IN} \geq \frac{2 \times P_{OUT} \times \frac{1}{60\,Hz}}{\left(V_{IN}^{\ 2} - V_{DROP}^{\ 2}\right)} \approx 364\,\mu F \tag{78}$$

Calculate high frequency input capacitor RMS current (I_{CINRMS}).

$$I_{CINRMS} = \sqrt{I_{PRMS1}^{\ 2} - \left(\frac{P_{OUT}}{V_{INMIN} \times a1}\right)^2} = 1.8\,A \tag{79}$$

To meet the input capacitance and RMS current requirements for this design we chose a 330-µF capacitor from Panasonic part number EETHC2W331EA.

$$C_{IN} = 330\,\mu F \tag{80}$$

This capacitor had a high frequency (ESR_{CIN}) of 150 mΩ this was measured with an impedance analyzer at both 120 and 200 kHz.

$$ESR_{CIN} = 0.150\,\Omega \tag{81}$$

Estimate C_{IN} power dissipation (P_{CIN}):

$$P_{CIN} = I_{CINRMS}^{\ 2} \times ESR_{CIN} = 0.5\,W \tag{82}$$

Recalculate remaining power budget:

$$P_{BUDGET} = P_{BUDGET} - P_{CIN} \approx 6.0\,W \tag{83}$$

There is roughly 6.0 W left in the power budget left for the current sensing network, and biasing the control device and all resistors supporting the control device.

Setting Up the Current Sense Network (CT, R_S, R_{RE}, D_A)

The CT chosen for this design had a turn's ratio (a2) of 100:1

$$a2 = \frac{I_P}{I_S} = 100 \tag{84}$$

Calculate nominal peak current (I_{P1}) at V_{INMIN}:

Peak primary current:

$$I_{P1} = \left(\frac{P_{OUT}}{V_{OUT} \times \eta} + \frac{\Delta I_{LOUT}}{2} \right) \frac{1}{a1} + \frac{V_{INMAX} \times D_{MAX}}{L_{MAG} \times f_s} \approx 3.3\,A \tag{85}$$

The voltage where peak current limit will trip.

$$V_P = 2\,V \tag{86}$$

Calculate current sense resistor (R_S) and leave 200 mV for slope compensation:

$$R_S = \frac{V_P - 0.2\,V}{\frac{I_{PEAK}}{a2} \times 1.1} \approx 49.9\,\Omega \tag{87}$$

Select a standard resistor for R_S:

$$R_S = 48.7\,\Omega \tag{88}$$

Estimate power loss for R_S:

$$P_{RS} = \left(\frac{I_{PRMS1}}{a2} \right)^2 \times R_S \approx 0.03\,W \tag{89}$$

Calculate maximum reverse voltage (V_{DA}) on D_A:

$$V_{DA} = V_P \frac{D_{CLAMP}}{1 - D_{CLAMP}} \approx 29.8\,V \tag{90}$$

Estimate D_A power loss (P_{DA}):

$$P_{DA} = \frac{P_{OUT} \times 0.6\,V}{V_{INMIN} \times \eta \times a2} \approx 0.01W \tag{91}$$

Calculate R_S reset resistor R_{RE}:

Resistor R_{RE} is used to reset the current sense transformer CT.

$$R_{RE} = 100 \times R_S = 4.87\,k\Omega \tag{92}$$

Resistor R_{LF} and capacitor C_{LF} form a low pass filter for the current sense signal (Pin 15). For this design we chose the following values. This filter has a low frequency pole (f_{LFP}) at 482 kHz. This should work for most applications but maybe adjusted to suit individual layouts and EMI present in the design.

$$R_{LF} = 1k\Omega \tag{93}$$

$$C_{LF} = 330\,pF \tag{94}$$

$$f_{LFP} = \frac{1}{2\pi f \times R_{LF} \times C_{LF}} = 482\,kHz \tag{95}$$

The UCC28950 VREF output (Pin 1) needs a high frequency bypass capacitor to filter out high frequency noise. This pin needs at least 1 µF of high frequency bypass capacitance (C_{BP1}). Please refer to figure 1 for proper placement.

$$C_{BP1} = 1\,\mu F \tag{96}$$

The voltage amplifier reference voltage (Pin 2, EA +) can be set with a voltage divider (R_A, R_B), for this design example we are going to set the error amplifier reference voltage (V1) to 2.5 V. Select a standard resistor value for R_B and then calculate resistor value R_A.

UCC28950 reference voltage:

$$V_{REF} = 5\,V \tag{97}$$

Set voltage amplifier reference voltage:

$$V1 = 2.5\,V \tag{98}$$

$$R_B = 2.37k\Omega \tag{99}$$

$$R_A = \frac{R_B \times (V_{REF} - V1)}{V1} = 2.37k\Omega \tag{100}$$

Voltage divider formed by resistor R_C and R_I are chosen to set the DC output voltage (V_{OUT}) at Pin 3 (EA-).

Select a standard resistor for R_C:

$$R_C = 2.37k\Omega \tag{101}$$

Calculate R_I:

$$R_I = \frac{R_c \times (V_{OUT} - V1)}{V1} \approx 9k\Omega \tag{102}$$

Then choose a standard resistor for R_I:

$$R_I = \frac{R_c \times (V_{OUT} - V1)}{V1} \approx 9.09k\Omega \tag{103}$$

Compensating the feedback loop can be accomplished by properly selecting the feedback components (R_F, C_Z and C_P). These components are placed as close to pin 3 and 4 as possible of the UCC28950.

Calculate load impedance at 10% load (R_{LOAD}):

$$R_{LOAD} = \frac{V_{OUT}^{2}}{P_{OUT} \times 0.1} = 2.4\,\Omega \tag{104}$$

Approximation of control to output transfer function ($G_{CO}(f)$) as a function of frequency:

$$G_{CO}(f) \approx \frac{\Delta V_{OUT}}{\Delta V_C} = a1 \times a2 \times \frac{R_{LOAD}}{R_S} \times \left(\frac{1 + 2\pi j \times f \times ESR_{COUT} \times C_{OUT}}{1 + 2\pi j \times f \times R_{LOAD} \times C_{OUT}} \right) \times \frac{1}{1 + \frac{S(f)}{2\pi \times f_{PP}} + \left(\frac{S(f)}{2\pi \times f_{PP}} \right)^2} \tag{105}$$

Double pole frequency of $G_{CO}(f)$:

$$f_{PP} \approx \frac{f_s}{4} = 50\,kHz \tag{106}$$

Angular velocity:

$$S(f) = 2\pi \times j \times f \tag{107}$$

Compensate the voltage loop with type 2 feedback network. The following transfer function is the compensation gain as a function of frequency ($G_C(f)$). Please refer to Figure 1 for component placement.

$$G_C(f) = \frac{\Delta V_C}{\Delta V_{OUT}} = \frac{2\pi j \times f \times R_F \times C_Z + 1}{2\pi j \times f \times (C_Z + C_P) R_I \left(\frac{2\pi j \times f \times C_Z \times C_P \times R_F}{C_Z + C_P} + 1 \right)} \tag{108}$$

Calculate voltage loop feedback resistor (R_F) based on crossing the voltage (f_C) loop over at a 10th of the double pole frequency (f_{PP}).

$$f_C = \frac{f_{PP}}{10} = 5\,kHz \tag{109}$$

$$R_F = \frac{R_I}{G_{CO}\left(\frac{f_{PP}}{10} \right)} \approx 27.9\,k\Omega \tag{110}$$

Select a standard resistor for R_F.

$$R_F \approx 27.4\,k\Omega \tag{111}$$

Calculate the feedback capacitor (C_Z) to give added phase at crossover.

$$C_Z = \frac{1}{2 \times \pi \times R_F \times \frac{f_C}{5}} \approx 5.8\,nF \tag{112}$$

Select a standard capacitance value for the design.

$$C_Z = 5.6\,nF \tag{113}$$

Put a pole at two times f_C.

$$C_P = \frac{1}{2 \times \pi \times R_F \times f_C \times 2} \approx 580\,pF \tag{114}$$

Select a standard capacitance value for the design.

$$C_P = 560\,pF \tag{115}$$

Loop gain as a function of frequency ($T_V(f)$) in dB.

$$T_V dB(f) = 20 \log\left(\left|G_C(f) \times G_{CO}(f)\right|\right) \tag{116}$$

Plot theoretical loop gain and phase to graphically check for loop stability (Figure 4). The theoretical loop gain crossed over at roughly 3.7 kHz with a phase margin of greater than 90 degrees.

NOTE: It is wise to check your loop stability of your final design with transient testing and/or a network analyzer and adjust the compensation ($G_C(f)$) feedback as necessary.

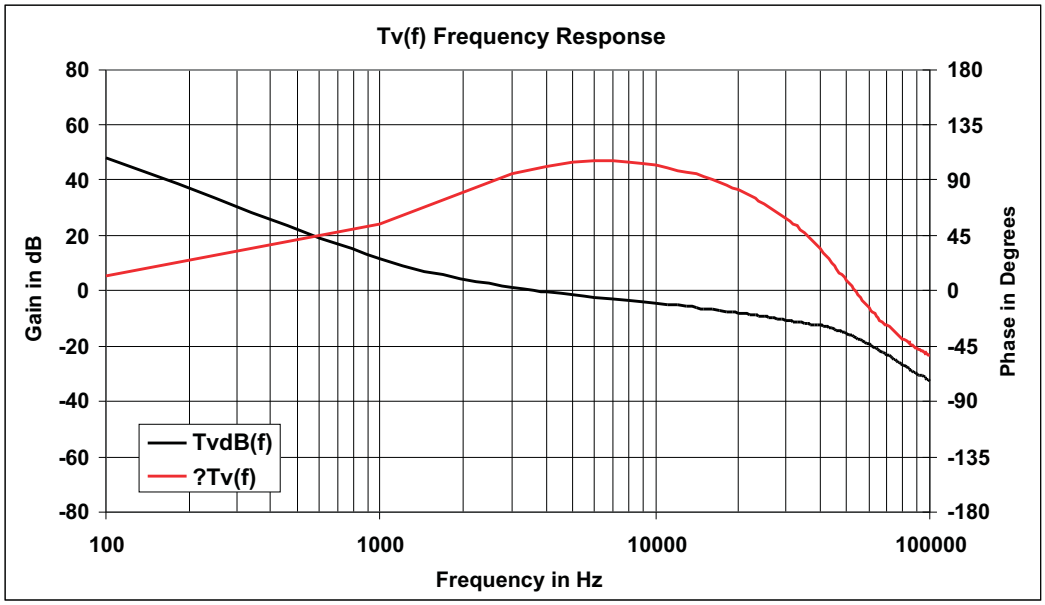

Figure 4. Loop Gain ($T_V dB(f)$), Loop Phase ($\theta T_V(f)$)

To limit over shoot during power up the UCC28950 has a soft-start function (SS, Pin 5) which in this application was set for a soft start time of 15 ms (t_{SS}).

$$t_{ss} = 15\,ms \tag{117}$$

$$C_{SS} = \frac{t_{SS} \times 25\,\mu A}{V1 + 0.55} \approx 123\,nF \tag{118}$$

Select a standard capacitor for the design.

$$C_{SS} = 150\,nF \tag{119}$$

This application note presents a fixed delay approach to achieving ZVS from 100% load down to 50% load. When the converter is operating below 50% load the converter will be operating in valley switching. In order to achieve zero voltage switching on switch node of QB_d, the turn-on (t_{ABSET}) delays of FETs QA and QB needs to be initially set based on the interaction of L_S and the theoretical switch node capacitance. The following equations are used to set t_{ABSET} initially.

Equate shim inductance to two times C_{OSS} capacitance:

$$2\pi \times f_R L_S = \frac{1}{2\pi \times f_R \times (2 \times C_{OSS\_QA\_AVG})} \tag{120}$$

Calculate tank frequency:

$$f_R = \frac{1}{2\pi\sqrt{L_S \times (2 \times C_{OSS\_QA\_AVG})}} \tag{121}$$

Set initial t_{ABSET} delay time and adjust as necessary.

NOTE: The 2.25 factor of the t_{ABSET} equation was derived from empirical test data and may vary based on individual design differences.

$$t_{ABSET} = \frac{2.25}{f_R \times 4} \approx 346\,ns \tag{122}$$

The resistor divider formed by R_{DA1} and R_{DA2} programs the t_{ABSET}, t_{CDSET} delay range of the UCC28950. Select a standard resistor value for R_{DA1}.

NOTE: t_{ABSET} can be programmed between 30 ns to 1000 ns.

$$R_{DA1} = 8.25\,k\Omega \tag{123}$$

The voltage at the ADEL input of the UCC28950 (V_{ADEL}) needs to be set with R_{DA2} based on the following conditions.

If t_{ABSET} > 155 ns set V_{ADEL} = 0.2 V, t_{ABSET} can be programmed between 155 ns and 1000 ns:

If $t_{ABSET} \leq$ 155 ns set V_{ADEL} = 1.8 V, t_{ABSET} can be programmed between 29 ns and 155 ns:

Based on V_{ADEL} selection, calculate R_{DA2}:

$$R_{DA2} = \frac{R_{DA1} \times V_{ADEL}}{5V - V_{ADEL}} \approx 344\,\Omega \tag{124}$$

Select the closest standard resistor value for R_{DA2}:

$$R_{DA2} = 348\,\Omega \tag{125}$$

Recalculate V_{ADEL} based on resistor divider selection:

$$V_{ADEL} = \frac{5\,V \times R_{DA2}}{R_{DA1} + R_{DA2}} = 0.202\,V \tag{126}$$

Resistor R_{DELAB} programs t_{ABSET}:

$$R_{DELAB} = \frac{(t_{ABSET} - 5\,ns)}{ns} \times \frac{(0.15\,V + V_{ADEL} \times 1.46) \times 10^3}{5} \times \frac{1}{1A} \approx 30.4\,k\Omega \tag{127}$$

Select a standard resistor value for the design:

$$R_{DELAB} = 30.1k\Omega \tag{128}$$

NOTE: Once you have a prototype up and running it is recommended you fine tune t_{ABSET} at light load to the peak and valley of the resonance between L_S and the switch node capacitance. In this design the delay was set at 10% load. Please refer to Figure 5.

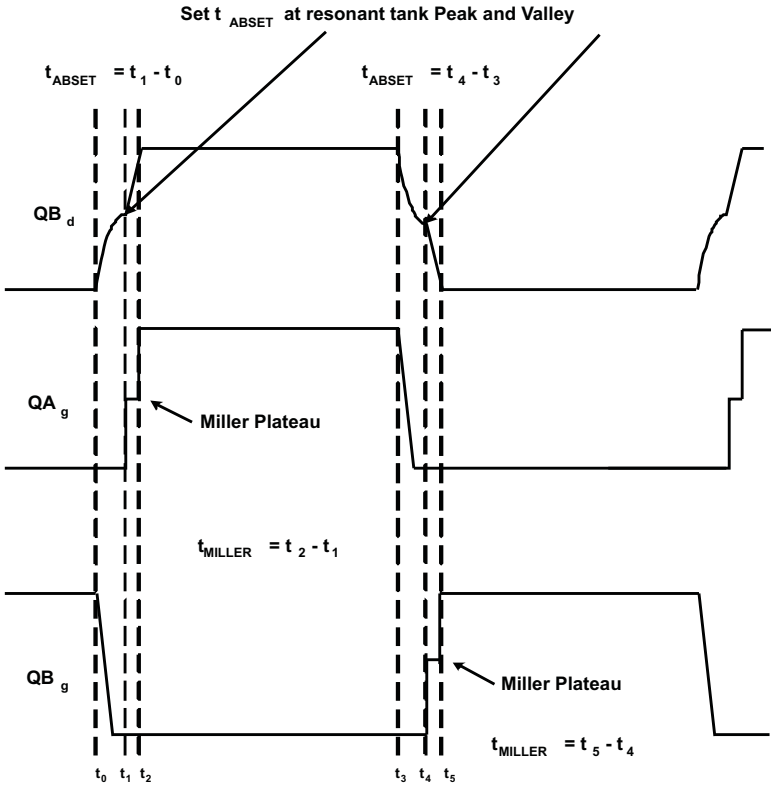

Figure 5. t_{ABSET} to Achieve Valley Switching at Light Loads

The initial starting point for the QC and QD turn on delays (t_{CDSET}) should be initially set for the same delay as the QA and QB turn on delays (Pin 6). The following equations program the QC and QD turn-on delays (t_{CDSET}) by properly selecting resistor R_{DELCD} (Pin 7).

$$t_{ABSET} = t_{CDSET} \tag{129}$$

Resistor R_{DELCD} programs t_{CDSET}:

$$R_{DELCD} = \frac{(t_{ABSET} - 5\,ns)}{ns} \times \frac{(0.15\,V + V_{ADEL} \times 1.46) \times 10^3}{5} \times \frac{1}{1A} \approx 30.4\,k\Omega \tag{130}$$

Select a standard resistor for the design:

$$R_{DELCD} = 30.1k\Omega \tag{131}$$

NOTE: Once you have a prototype up and running it is recommended to fine tune t_{CDSET} at light load. In this design the CD node was set to valley switch at roughly 10% load. Please refer to Figure 6. Obtaining ZVS at lighter loads with switch node QD_d is easier due to the reflected output current present in the primary of the transformer at FET QD and QC turnoff/on. This is because there was more peak current available to energize L_S before this transition, compared to the QA and QB turnoff/on.

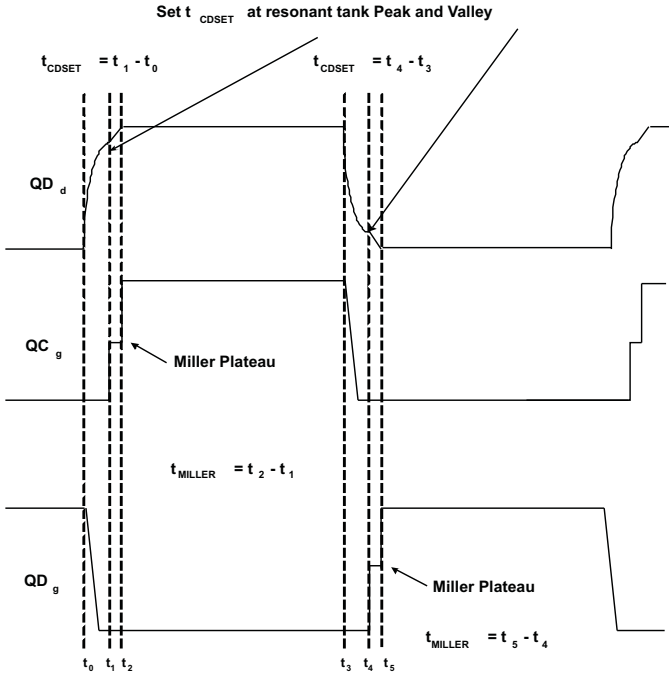

Figure 6. t_{CDSET} to Achieve Valley Switching at Light Loads

There is a programmable delay for the turnoff of FET QF after FET QA turnoff (t_{AFSET}) and the turnoff of FET QE after FET QB turnoff (t_{BESET}). A good place to set these delays is 50% of t_{ABSET}. This will ensure that the appropriate synchronous rectifier turns off before the AB ZVS transition. If this delay is too large it will cause OUTE and OUTF not to overlap correctly and it will create excess body diode conduction on FETs QE and QF.

$$t_{AFSET} = t_{BESET} = t_{ABSET} \times 0.5 \tag{132}$$

The resistor divider formed by R_{CA1} and R_{CA2} programs the t_{AFSET} and t_{BESET} delay range of the UCC28950. Select a standard resistor value for R_{CA1}.

NOTE: t_{EFSET} and t_{BESET} can be programmed between 32 ns to 1100 ns.

$$R_{CA1} = 8.25\,k\Omega \tag{133}$$

The voltage at the A_{DELEF} pin of the UCC28950 (V_{ADELEF}) needs to be set with R_{CA2} based on the following conditions.

If t_{AFSET} < 170 ns set V_{ADEL} = 0.2 V, t_{ABSET} can be programmed between 32 ns and 170 ns:

If t_{ABSET} > or = 170 ns set V_{ADEL} = 1.7 V, t_{ABSET} can be programmed between 170 ns and 1100 ns:

Based on V_{ADELEF} selection, calculate R_{CA2}:

$$R_{CA2} = \frac{R_{CA1} \times V_{ADELEF}}{5\,V - V_{ADELEF}} \approx 4.25\,k\Omega \tag{134}$$

Select the closest standard resistor value for R_{CA2}:

$$R_{CA2} = 4.22\,k\Omega \tag{135}$$

Recalculate V_{ADELEF} based on resistor divider selection:

$$V_{ADELEF} = \frac{5\,V \times R_{CA2}}{R_{CA1} + R_{CA2}} = 1.692\,V \tag{136}$$

The following equation was used to program t_{AFSET} and t_{BESET} by properly selecting resistor R_{DELEF}.

$$R_{DELEF} = \frac{\left(t_{AFSET} \times 0.5 - 4\,ns\right)}{ns} \times \frac{\left(2.65\,V - V_{ADELEF} \times 1.32\right) \times 10^3}{5} \times \frac{1}{1A} \approx 14.1\,k\Omega \tag{137}$$

A standard resistor was chosen for the design.

$$R_{DELEF} = 14\,k\Omega \tag{138}$$

Resistor R_{TMIN} programs the minimum duty cycle on time (t_{MIN}) that the UCC28950 (Pin 9) can demand before entering burst mode. If the UCC28950 controller tries to demand a duty cycle on time of less than t_{MIN} the power supply will go into burst mode operation. Please see the UCC28950 data sheet for details regarding burst mode. For this design we set the minimum on time to 100 ns.

$$t_{MIN} = 100\,ns \tag{139}$$

The minimum on time is set by selecting R_{TMIN} with the following equation.

$$R_{TMIN} = \frac{(t_{MIN} - 15\,ns) \times 10^3}{6.6\,s} \approx 12.9\,k\Omega \tag{140}$$

A standard resistor value is then chosen for the design.

$$R_{TMIN} = 13\,k\Omega \tag{141}$$

There is a pin that is provided for setting up the converter switching frequency (Pin 10). The frequency can be selected by adjusting timing resistor R_T.

$$R_T = \left(\frac{2.5 \times 10^6 \frac{\Omega Hz}{V}}{\frac{f_S}{2}} - \frac{\Omega}{V} \right) \times (V_{REF} - 2.5\,V) \times 2.5 \times 10^3 \approx 60\,k\Omega \tag{142}$$

Select a standard resistor for the design.

$$R_T = 61.9\,k\Omega \tag{143}$$

The UCC28950 also provides slope compensation for peak current mode control (Pin 12). This can be set by setting R_{SUM} with the following equations. The following equations will calculate the required amount of slope compensation (V_{SLOPE}) that is needed for loop stability.

NOTE: The change in magnetizing current on the primary dIL_{MAG} contributes to slope compensation.

$$\Delta I_{LMAG} = \frac{V_{IN}(1 - D_{TYP})}{L_{MAG} \times f_s} = 234\,mA \tag{144}$$

To help improve noise immunity V_{SLOPE} is set to have a total slope that will equal 10% of the maximum current sense signal (0.2 V) over one inductor switching period.

$$V_{SLOPE1} = 0.2\,V \times f_S = \frac{0.04\,V}{\mu s} \tag{145}$$

$$V_{SLOPE2} = \frac{\left(\frac{dIL_{OUT}}{a1 \times 2} - dIL_{MAG}\right) \times R_S \times f_S}{a2 \times (1 - D_{TYP})} = \frac{1mV}{\mu s} \tag{146}$$

If $V_{SLOPE2} < V_{SLOPE1}$ set $V_{SLOPE} = V_{SLOPE1}$

If $V_{SLOPE2} \geq V_{SLOPE1}$ set $V_{SLOPE} = V_{SLOPE2}$

$$R_{SUM} = \frac{2.5\,V \times 10^3\,\Omega}{V_{SLOPE} \times 0.5\,\mu s} \approx 125.4\,k\Omega \tag{147}$$

Select a standard resistor for R_{SUM}.

$$R_{SUM} = 127\,k\Omega \tag{148}$$

To increase efficiency at lighter loads the UCC28950 is programmed (Pin 12, DCM) under light load conditions to turn off the synchronous FETs on the secondary side of the converter (Q_E and Q_F). This threshold is programmed with resistor divider formed by R_E and R_G. This DCM threshold needs to be set at a level before the inductor current goes discontinues. The following equation sets the synchronous rectifiers to turnoff at roughly 15% load current.

$$V_{RS} = \frac{\left(\frac{P_{OUT} \times 0.15}{V_{OUT}} + \frac{\Delta I_{LOUT}}{2}\right) \times R_S}{a1 \times a2} = 0.29\,V \tag{149}$$

Select a standard resistor value for R_G.

$$R_G = 1k\Omega \tag{150}$$

Calculate resistor value R_E.

$$R_E = \frac{R_G\left(V_{REF} - V_{RS}\right)}{V_{RS}} \approx 16.3\,k\Omega \tag{151}$$

Select a standard resistor value for this design

$$R_E = 16.9\,k\Omega \tag{152}$$

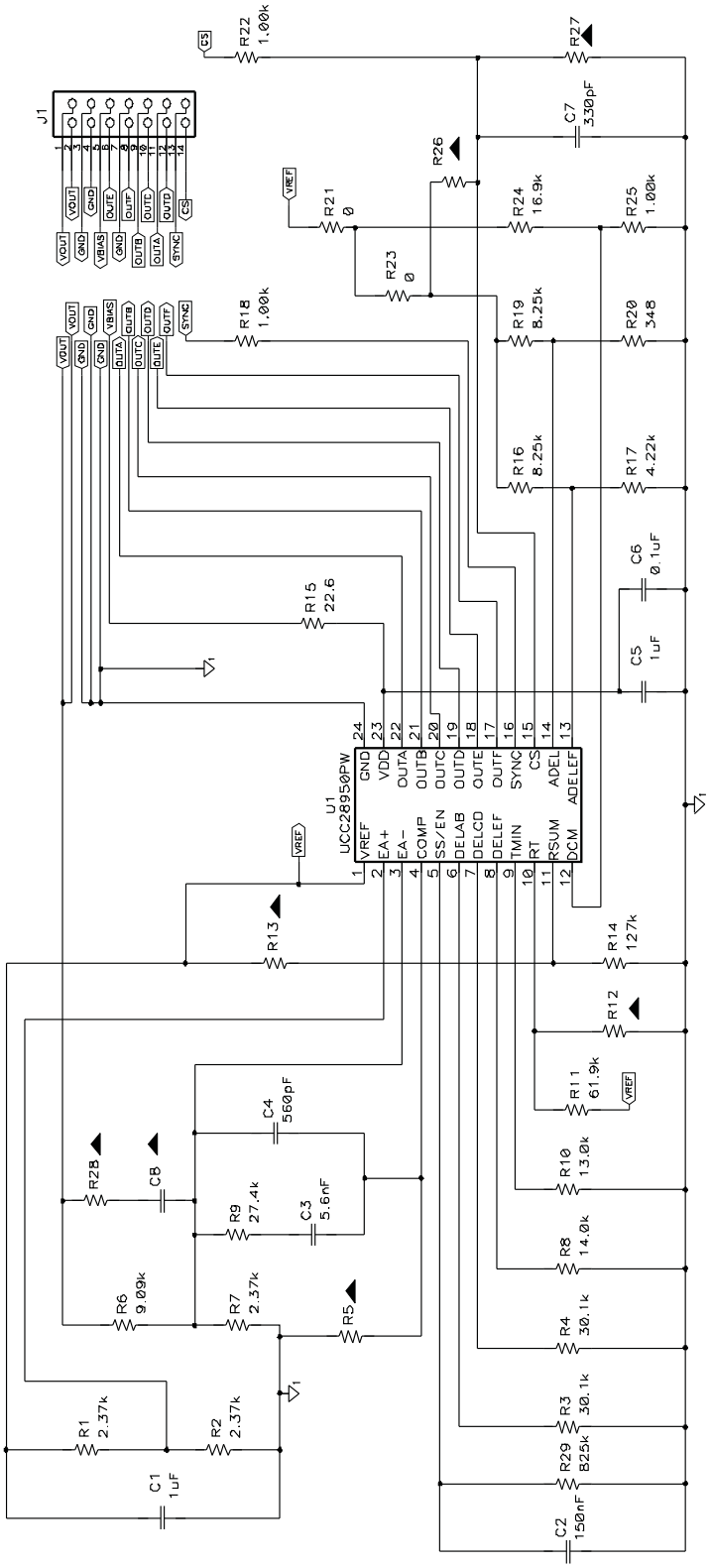

Figure 7. Daughter Board Schematic

NOTE: Black triangles designate not populated.

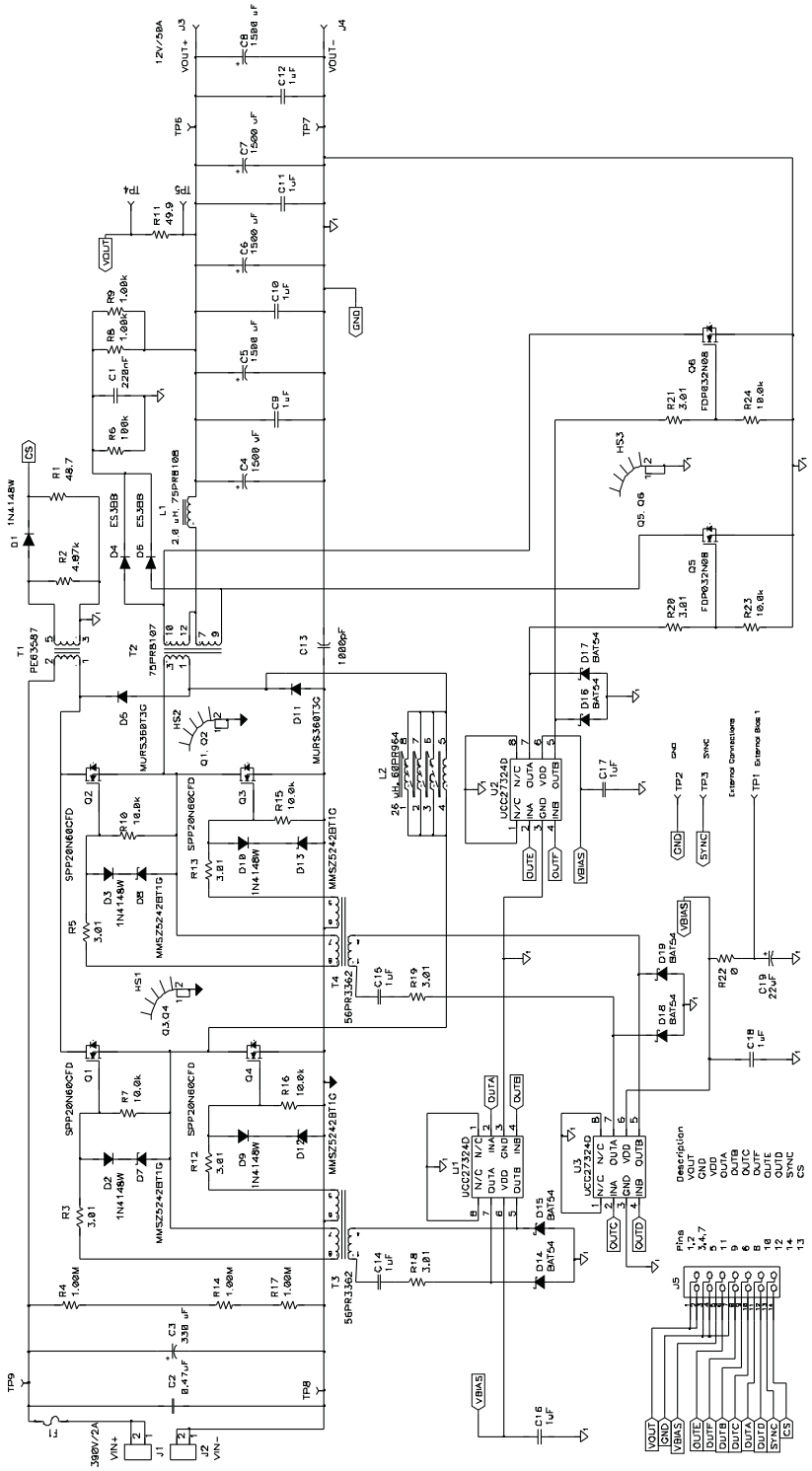

Figure 8. Power Stage Schematic

NOTE: It is recommended to use an RCD clamp to protect the output synchronous FETs from over voltage due to switch node ringing. This RCD clamp is formed by diodes D4, D6 and resistor R6, R8 and R9 and capacitor C1 in the power stage schematic, .

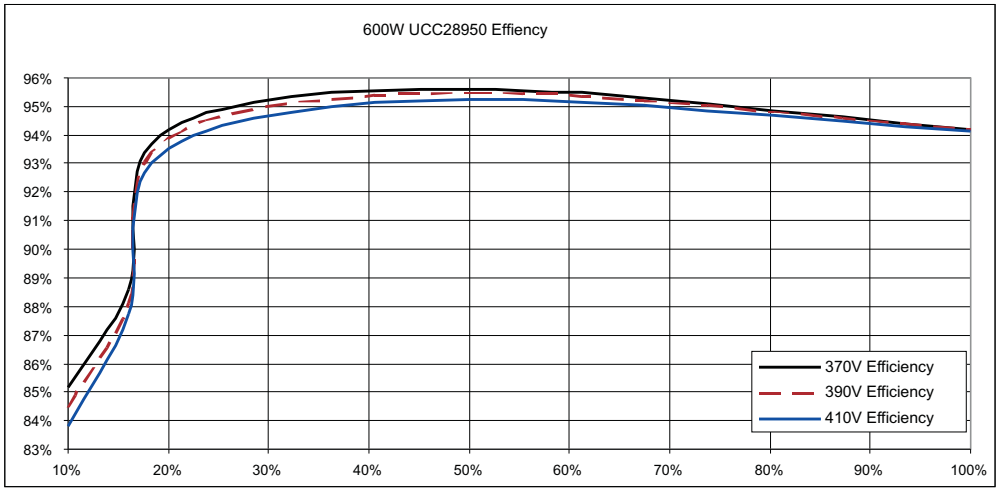

Figure 9. 600-W Phase Shifted Full Bridge Efficiency

Full bridge gate drives and primary switch nodes (QB_d and QD_d) at V_{IN} = 390 V, I_{OUT} = 5 A.

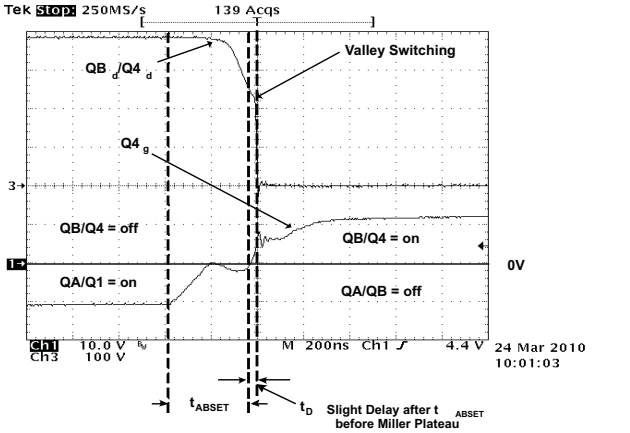

Figure 10. $Q4_g$ $Q4_d$, V_{IN} = 390 V, I_{OUT} = 5 A

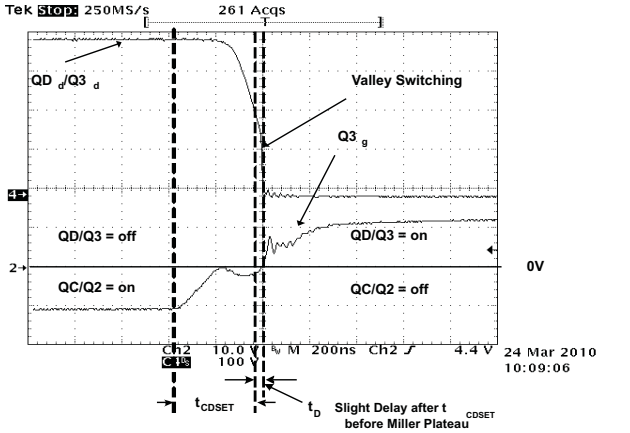

Figure 11. $Q3_g$ $Q3_d$, V_{IN} = 390 V, I_{OUT} = 5 A

NOTE: The gate drives look slightly different than Figure 5 and Figure 6. This is because they were driven with 1:2 gate drive transformers instead of 1:1. At 10% load the primary switch nodes were valley switching

Full bridge gate drives and switch nodes at V_{IN} = 390 V, I_{OUT} = 10 A

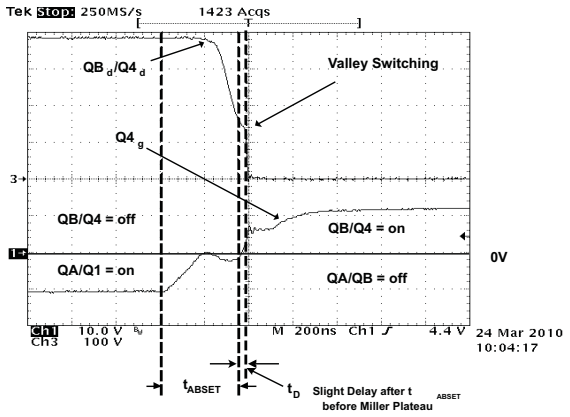

Figure 12. $Q4_g$ $Q4_d$, V_{IN} = 390 V, I_{OUT} = 10 A

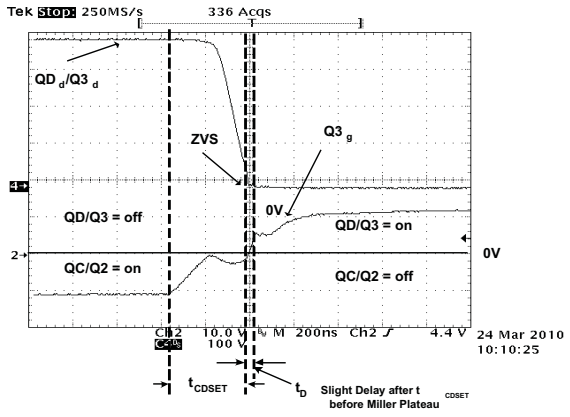

Figure 13. $Q3_g$ $Q3_d$, V_{IN} = 390 V, I_{OUT} = 10 A

NOTE: Switch node $QB_d/Q4_d$ is valley switching and node $QD_d/Q3_d$ has achieved ZVS. Please refer to Figure 12 and Figure 13. It is not uncommon for switch node $QD_d/Q3_d$ to obtain ZVS before $QB_d/Q4_d$. This is because during the $QD_d/Q3_d$ switch node voltage transition, the reflected output current provides immediate energy for the LC tanking at the switch node. Where at the $QB_d/Q4_d$ switch node transition the primary has been shorted out by the high side or low side FETs in the H bridge. This transition is dependent on the energy stored in L_S and L_{LK} to provide energy for the LC tanking at switch node $QB_d/Q4_d$ making it take longer to achieve ZVS.

Full bridge gate drives and switch nodes at V_{IN} = 390 V, I_{OUT} = 25 A

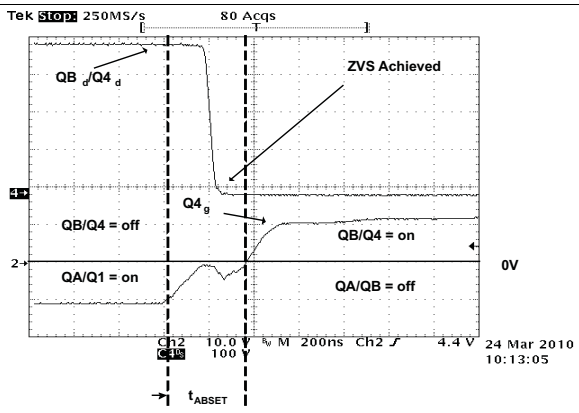

Figure 14. $Q4_g$ $Q4_d$, V_{IN} = 390 V, I_{OUT} = 25 A

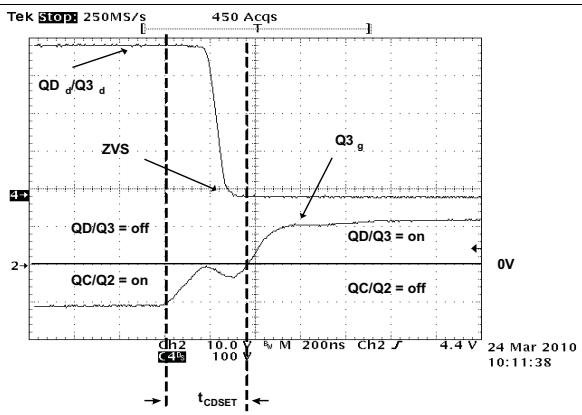

Figure 15. $Q3_g$ $Q3_d$, V_{IN} = 390 V, I_{OUT} = 25 A

NOTE: When the converter is running at 25 A both switch nodes are operating into zero voltage switching (ZVS). It is also worth mentioning that there is no evidence of the gate miller plateau during gate driver switching. This makes sense because the voltage across the drain and source of FETs QA through QD has already transition before the gate drives have transitioned.

Full bridge gate drives and switch nodes at V_{IN} = 390 V, I_{OUT} = 50 A

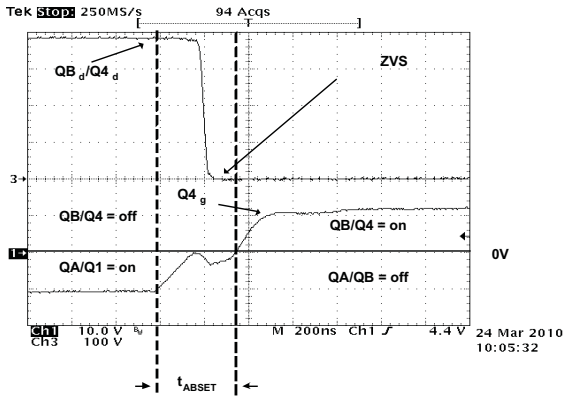

Figure 16. $Q4_g$ $Q4_d$, V_{IN} = 390 V, I_{OUT} = 25 A

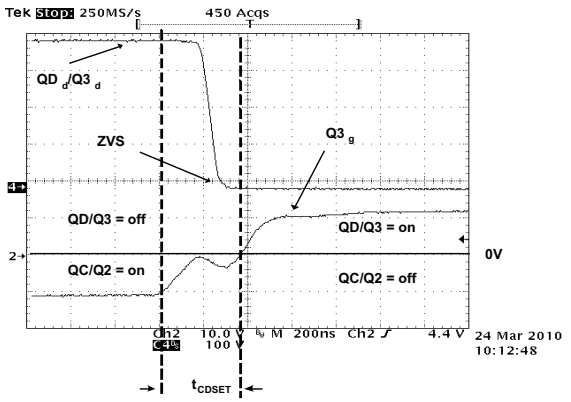

Figure 17. $Q3_g$ $Q3_d$, V_{IN} = 390 V, I_{OUT} = 25 A

NOTE: ZVS was maintained from 50% to 100% output power.

References

1. Bill Andreycak, "*Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller*" Unitrode Application Note SLUA107, 9/5/1999
2. Lazlo Balogh, "*Design and Application Guide for High Speed MOSFET Gate Drive*" Unitrode Power Supply Design Seminar 1400, Topic 2, 2001

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